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Abstract
The representation of audio, image and video signals involves a vast amount of data, so signal compression is indispensable. Recently, variable length code (VLC) has been widely used in multimedia and lossless coding compression. This thesis describes an efficient class-based VLC encoder/decoder and its VLSI architecture. It takes advantage of logic optimization techniques, and achieves high throughput. The computation complexity of the proposed VLC is quite low and its memory requirement is small. Hence, it is easily implemented by VLSI and very suitable for real-time applications on many international image standards, such as JPEG, H.261 and MPEG.

An efficient VLSI architecture for the VLC is designed, then is synthesized with the standard-cell from TSMC's cell library. The chip areas are about 1646 1646 and 1646 1646 for the encoder and the decoder respectively, The gate counts are about 2520 and 1896. It can achieve about 50Mega symbols/sec encoding/decoding rate. Finally, a demo system is built by integrating an Altera FPGA chip implemented the proposed VLC with an 8051 microprocessor to verify the performance of our VLC in JPEG standard.
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